Fig. 1

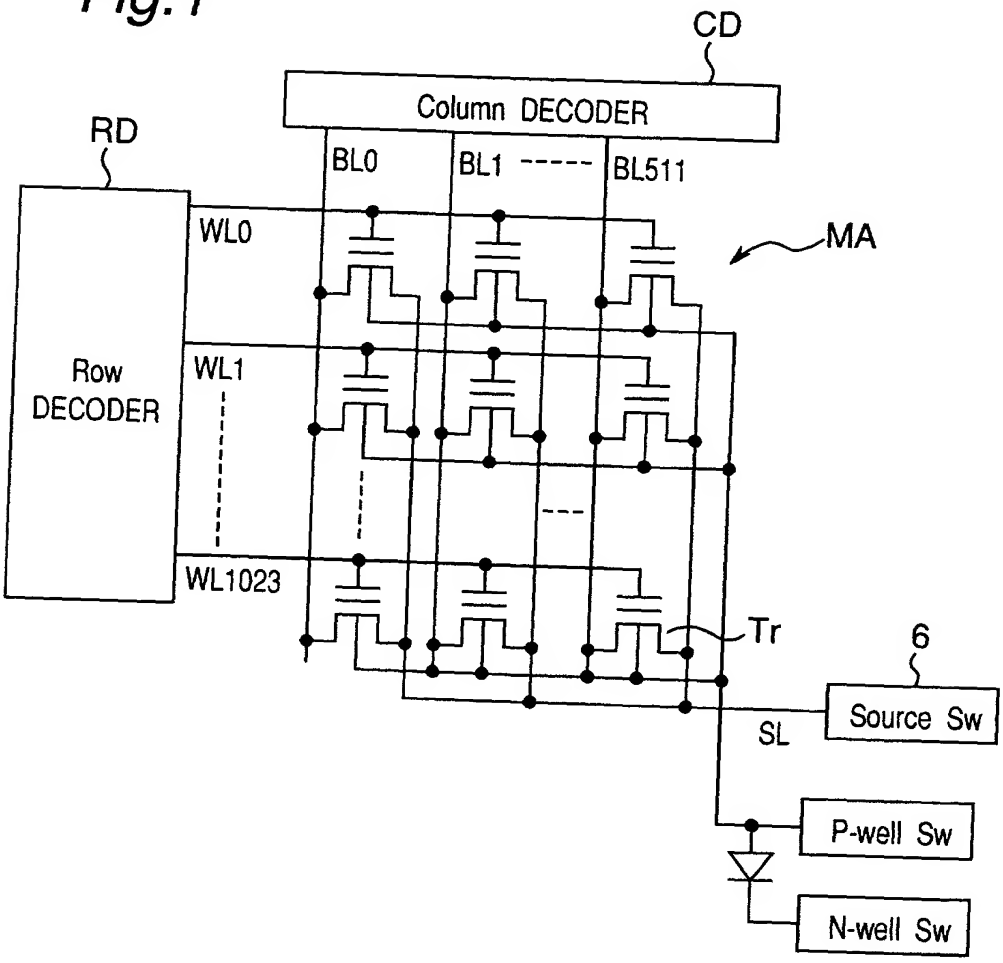

CD
Column DECODER
RD
BL0
BL1
BL511
WL0
MA
Row
DECODER
WL1
WL1023
Tr
6
Source Sw
SL
P-well Sw
N-well Sw

Fig.2

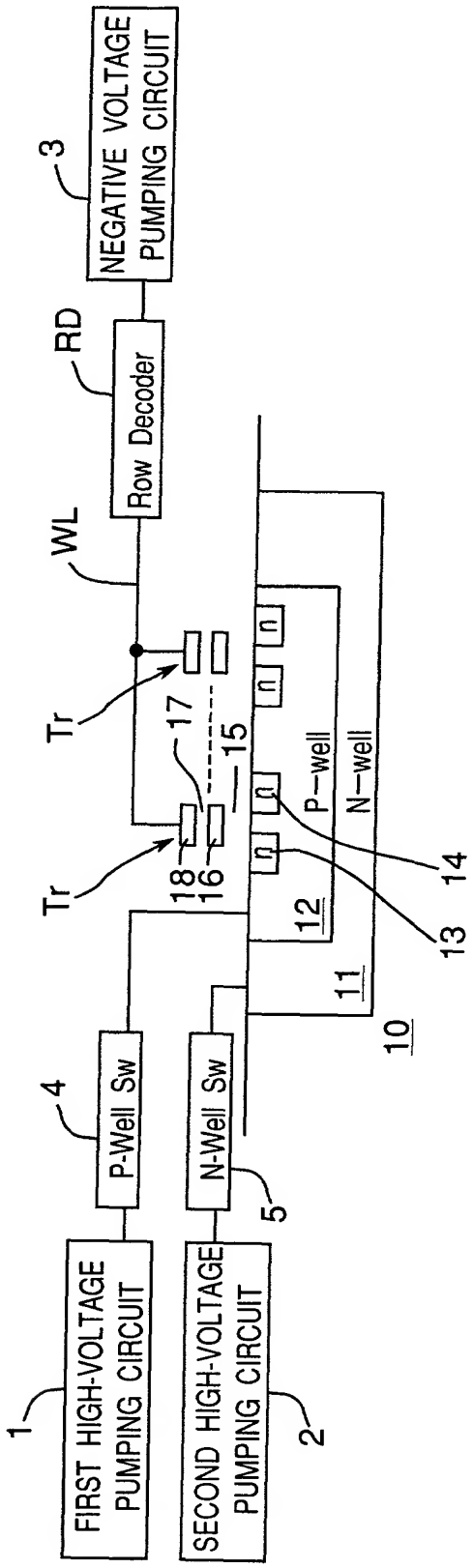


Fig.3

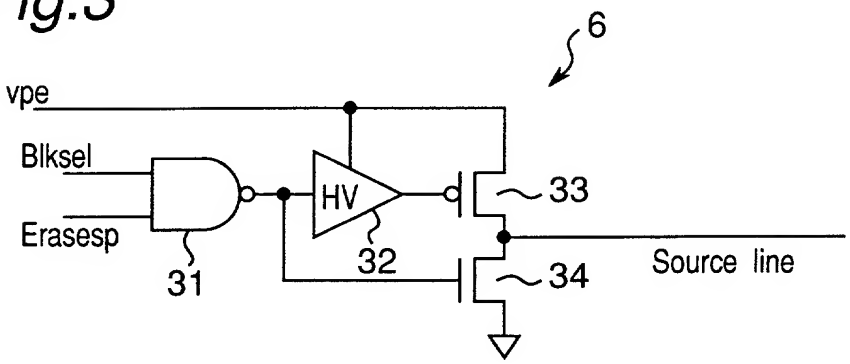


Fig.4

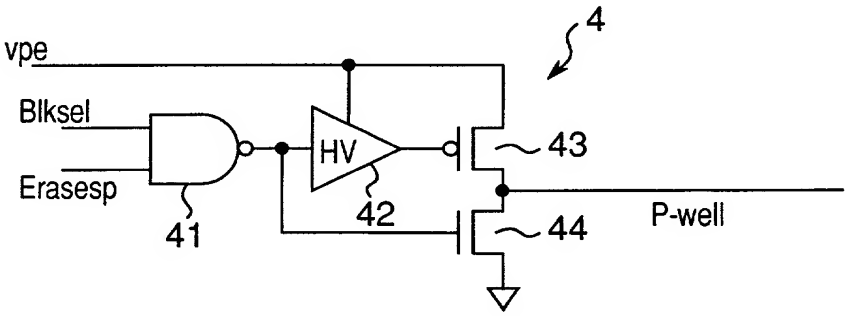


Fig.5

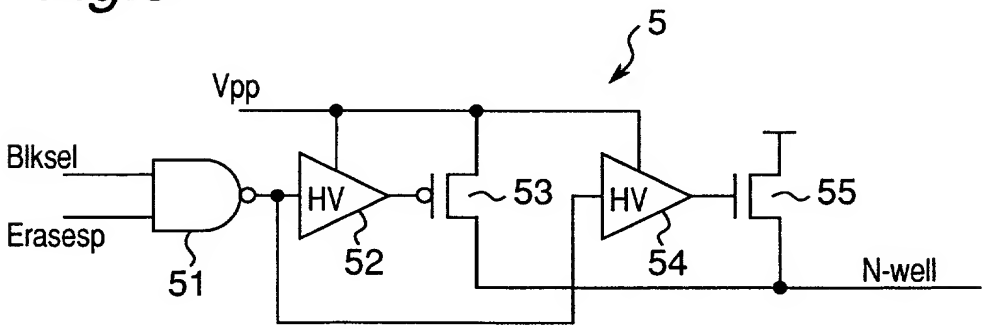


Fig.6

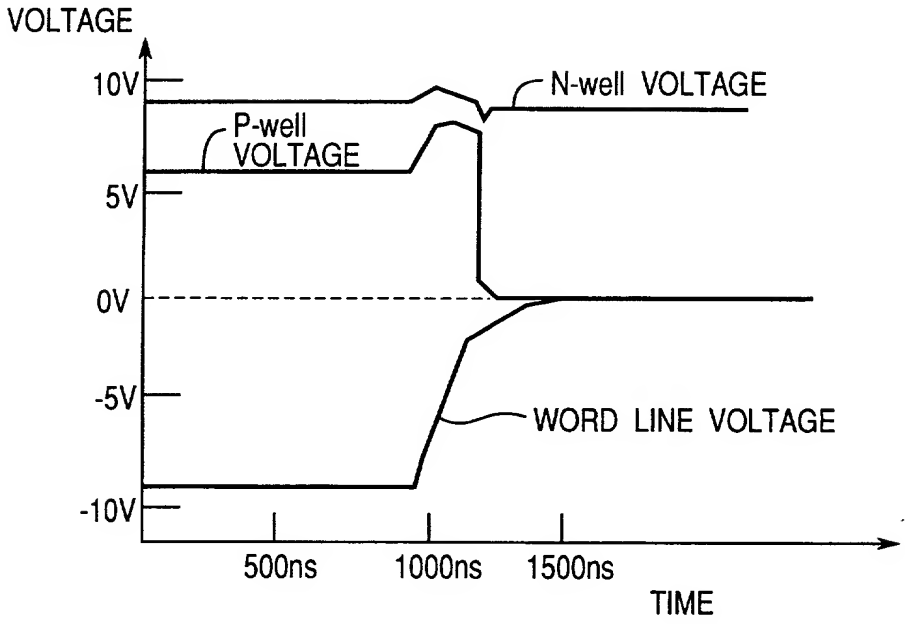
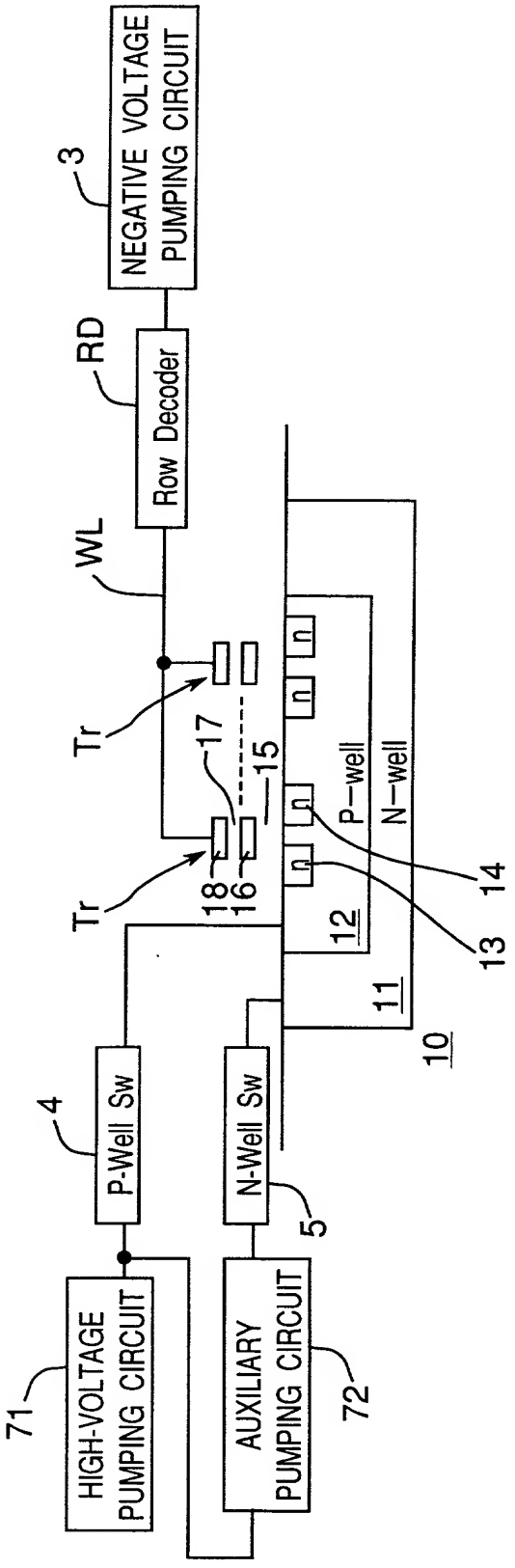

VOLTAGE
10V
5V
0V
-5V
-10V
N-well VOLTAGE
P-well
VOLTAGE
WORD LINE VOLTAGE
500ns
1000ns
1500ns
TIME

Fig.7



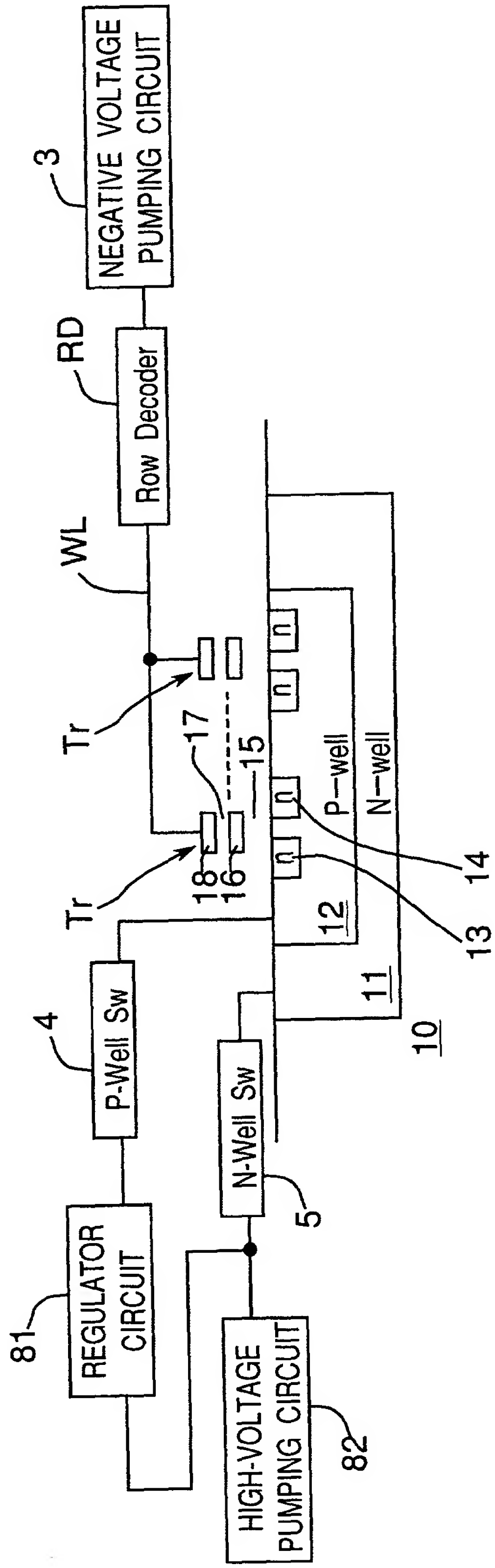

NEGATIVE VOLTAGE PUMPING CIRCUIT
3
Row Decoder
RD
WL
Tr
Tr
17
15
18
16
P—well
N—well
n
n
n
n
14
13
12
11
10
P-Well Sw
4
N-Well Sw
5
REGULATOR CIRCUIT
81
HIGH-VOLTAGE PUMPING CIRCUIT
82

Fig.8

Fig.9

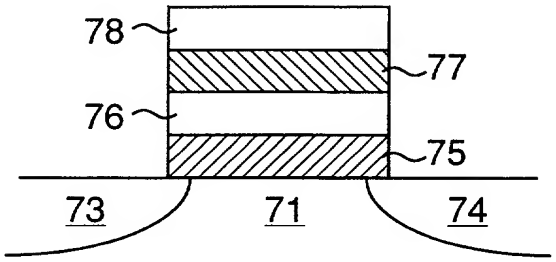
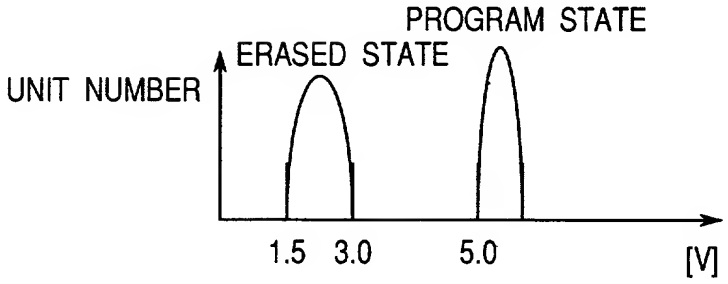

78
77
76
75
73
71
74

Fig.10


PROGRAM STATE
ERASED STATE
UNIT NUMBER
1.5
3.0
5.0
[V]

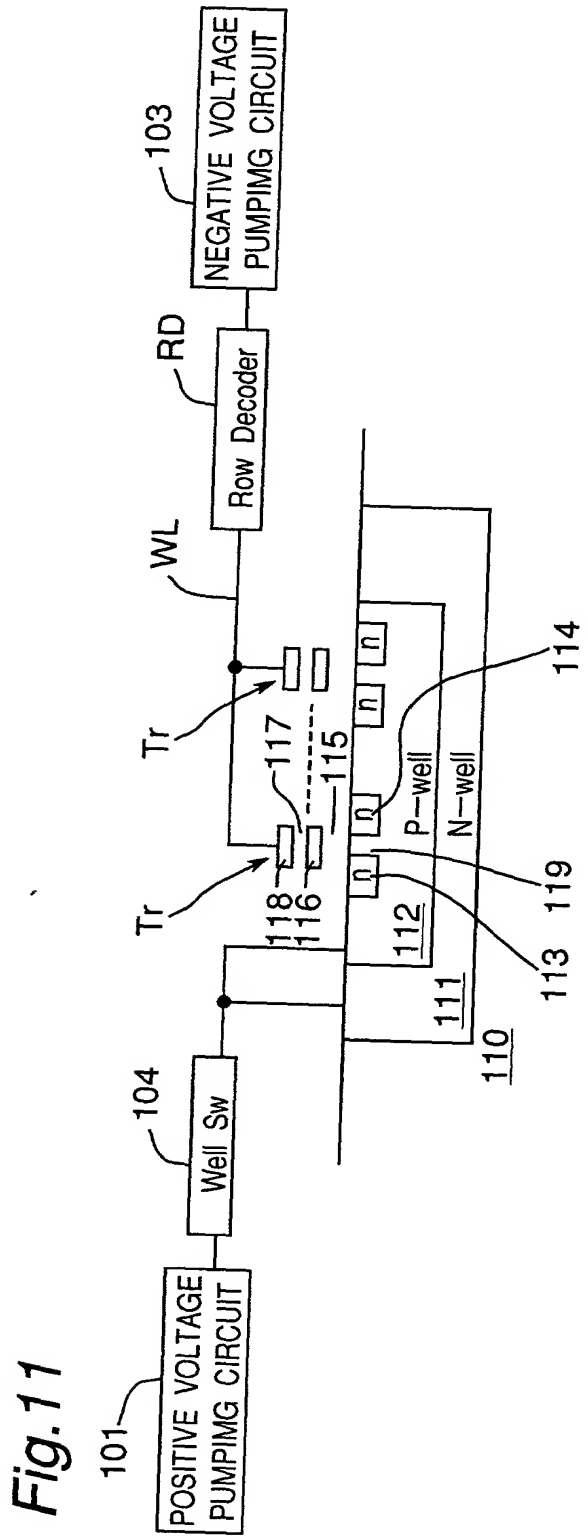


Fig.11

Fig. 12

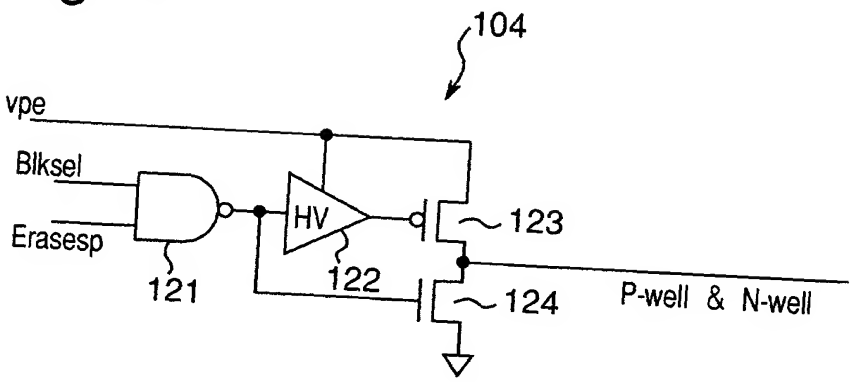


Fig.13

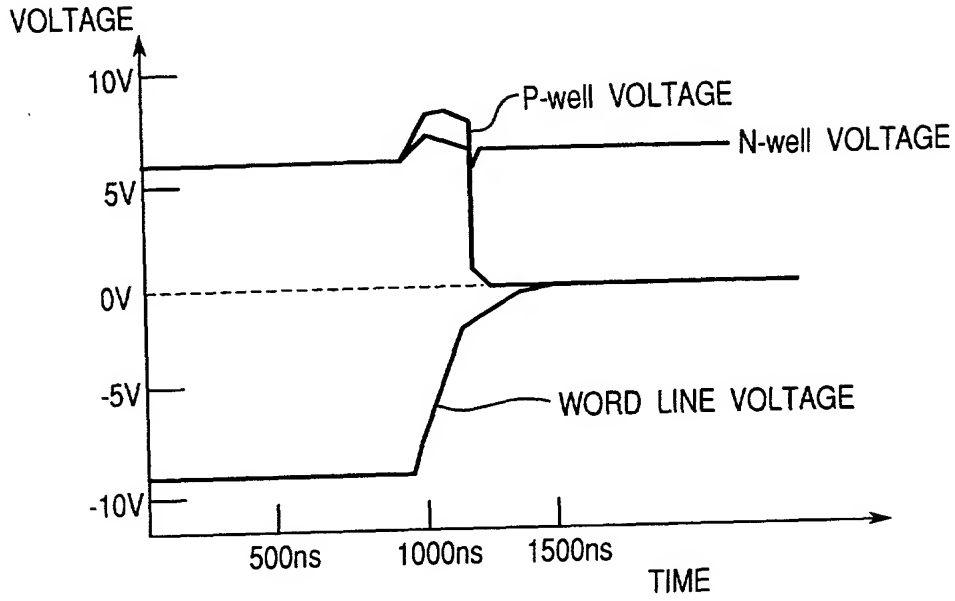
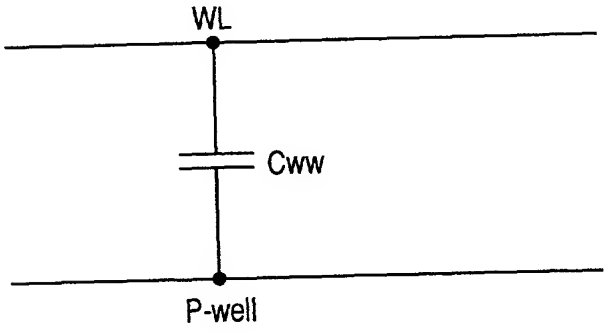

VOLTAGE
10V
5V
0V
-5V
-10V
P-well VOLTAGE
N-well VOLTAGE
WORD LINE VOLTAGE
500ns
1000ns
1500ns
TIME

Fig.14


WL
Cww
P-well